

FIG. 1

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The diagram illustrates a hierarchical bus architecture. At the top level, there are three **ROOT BUS**s: **ROOT BUS 0**, **ROOT BUS 1**, and **ROOT BUS 2**. **HOST CPU** (14) connects to **HOST MEMORY (HDRAM)** (16) via **HOST BRIDGE RB0**. **HOST MEMORY (HDRAM)** (16) connects to **CACHE** (18) via **HOST BRIDGE RB1**. **CACHE** (18) connects to the **HOST BUS** (12). The **HOST BUS** (12) connects to **HOST/PCI BRIDGE RB2**, which in turn connects to **HOST/PCI BRIDGE RB2**. **HOST/PCI BRIDGE RB2** connects to **LEGACY DEVICES** (30), **BR1**, **BR2**, **BR3**, **BR4**, **BR5**, **BR6**, **BR7**, **BR8**, **BR9**, **BR10**, **BR11**, **BR12**, **BR13**, and **BR14**. **BR1** connects to **LB 1-28**. **LB 1-28** connects to **BR2**. **BR2** connects to **BR3**. **BR3** connects to **LEGACY DEVICES** (30). **BR4** connects to **BR5**. **BR5** connects to **D**. **BR6** connects to **D**. **BR7** connects to **D**. **BR8** connects to **D**. **BR9** connects to **D**. **BR10** connects to **D**. **BR11** connects to **D**. **BR12** connects to **D**. **BR13** connects to **D**. **BR14** connects to **D**. **BR1** also connects to **B1**, **BR2** connects to **B2**, **BR3** connects to **B3**, **BR4** connects to **B4**, **BR5** connects to **B5**, **BR6** connects to **B6**, **BR7** connects to **B7**, **BR8** connects to **B8**, **BR9** connects to **B9**, **BR10** connects to **B10**, **BR11** connects to **B11**, **BR12** connects to **B12**, **BR13** connects to **B13**, and **BR14** connects to **B14**.

FIG. 2

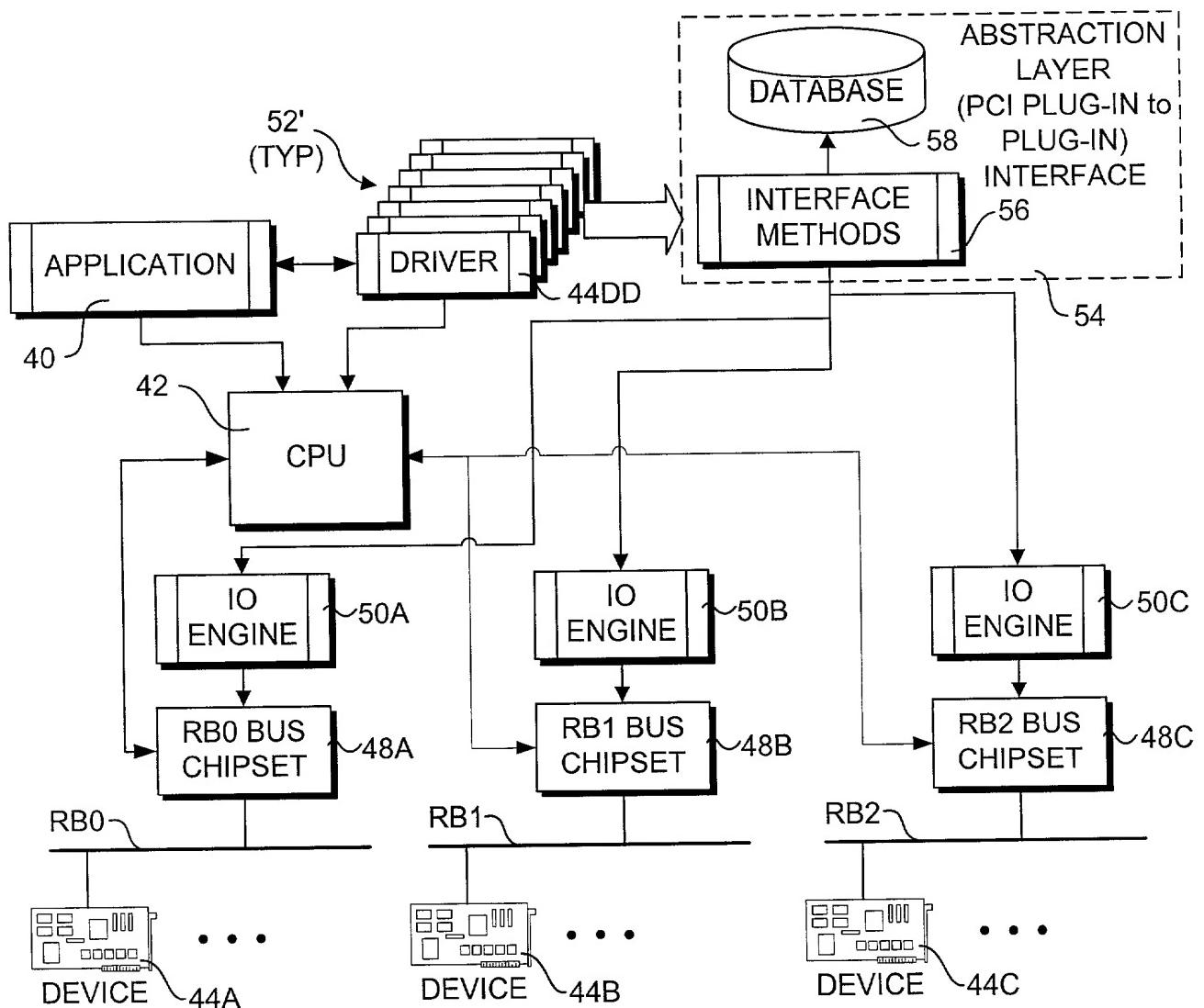
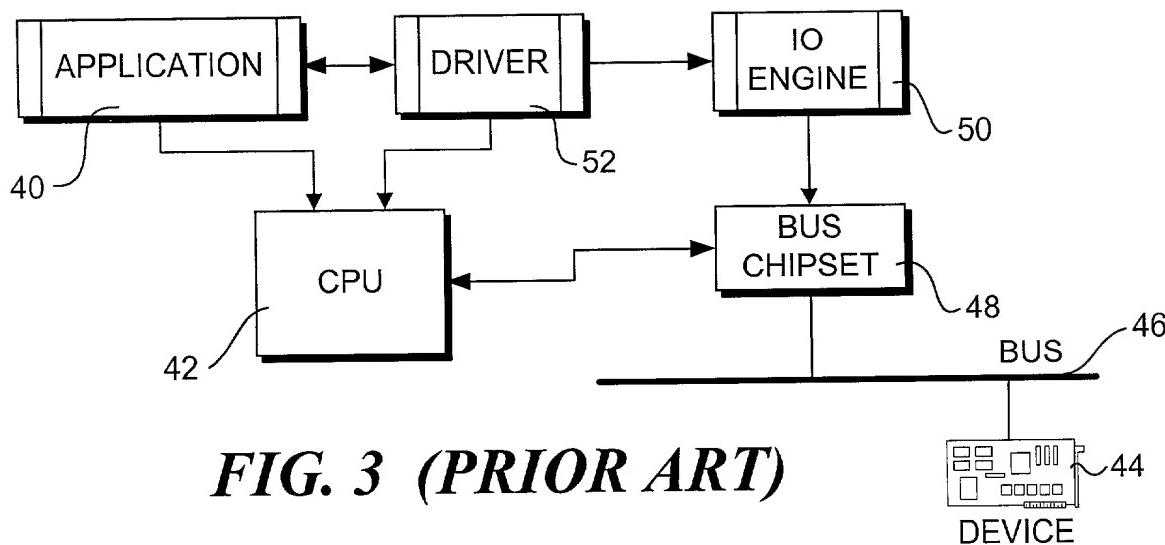


FIG. 5

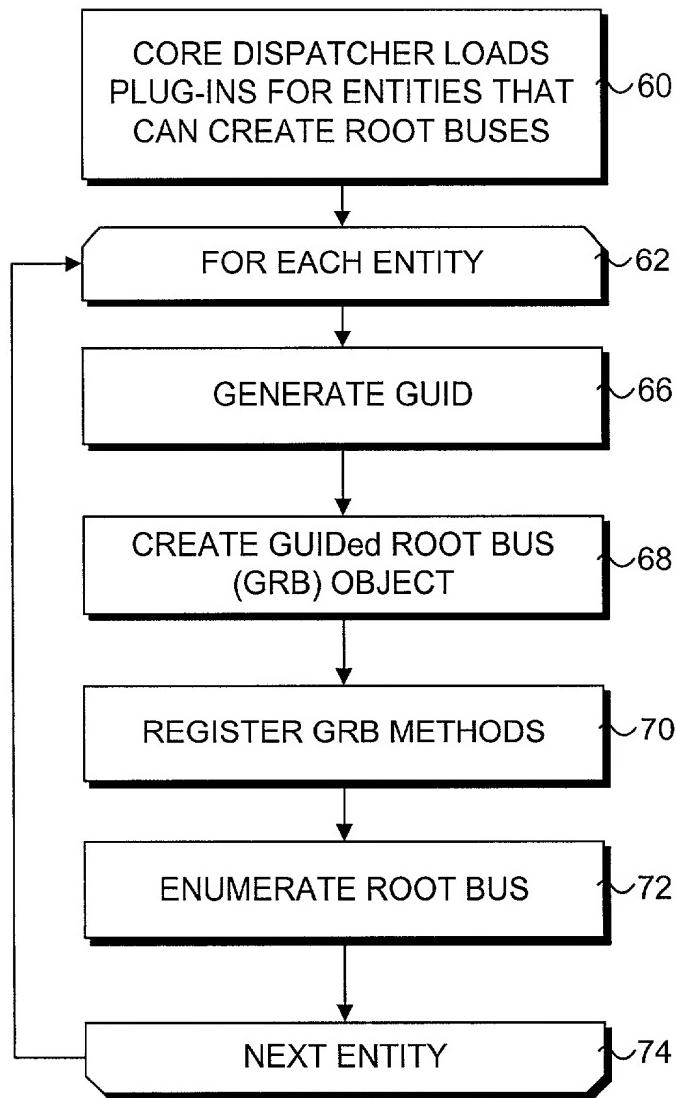
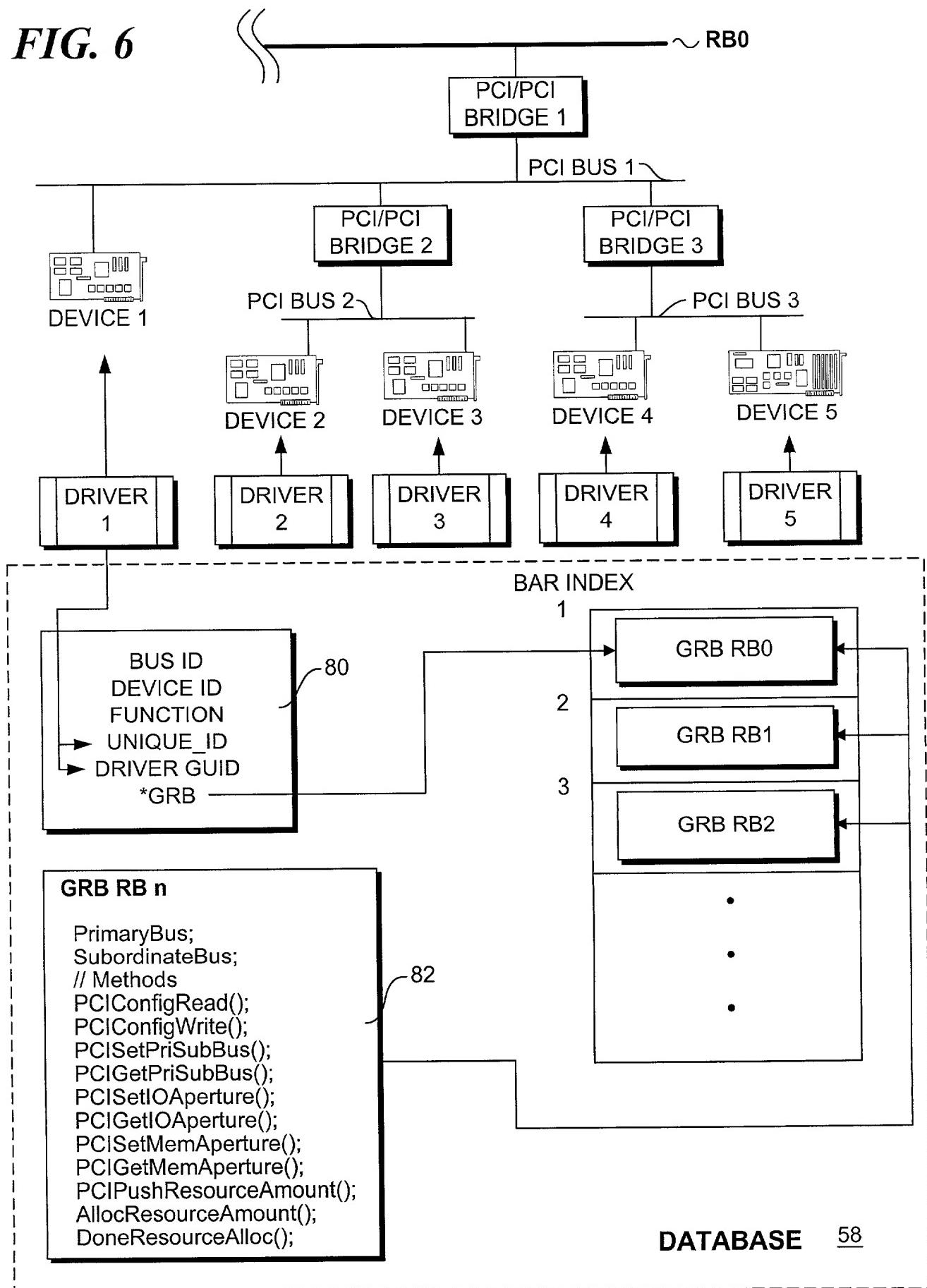


FIG. 6



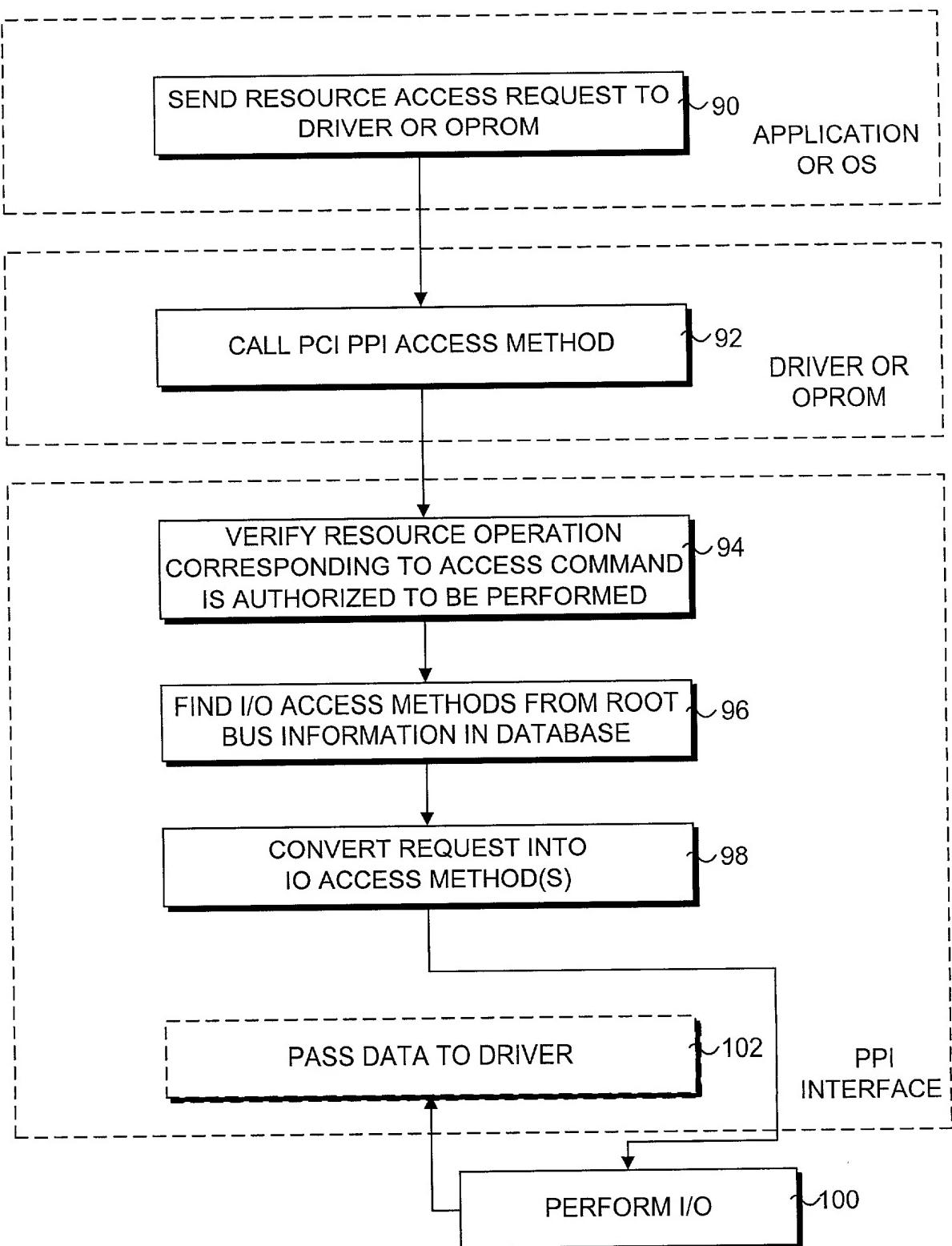


FIG. 7

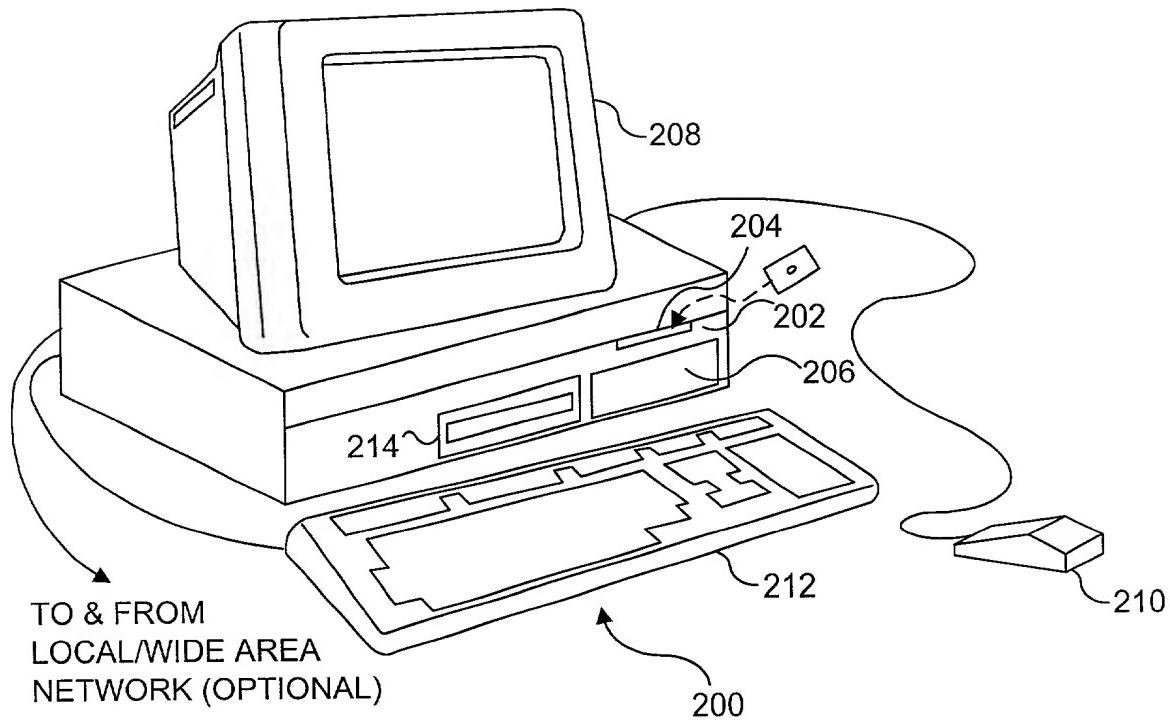


FIG. 8